

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)
2. (previously presented) A logic circuit comprising:
 - a first series of logic elements, each logic element having a look-up table and a dedicated adder to implement an arithmetic mode in the logic element;
 - a carry chain connecting the first series of logic element;
 - an initialization circuit connected to the carry chain to initialize the carry chain; and
 - a multiplexer connected to a selection signal, the multiplexer having:
 - a first input connected to a carry in signal;
 - a second input connected to a power supply; and
 - an output connected to the carry chain.
3. (previously amended) A logic circuit comprising;
 - a first series of logic elements, each logic element having a look-up table and a dedicated adder to implement an arithmetic mode in the logic element;
 - a carry chain connecting the first series of logic element;
 - an initialization circuit connected to the carry chain to initialize the carry chain;
 - a first path connecting the first series of logic element; and
 - a second path connecting a second series of logic elements,wherein the logic elements in the first series are a subset of the logic elements in the second series.
4. (Original) The logic circuit of claim 3, further comprising;
 - a first multiplexer having a first input and a second input,

wherein when the first input is selected, a carry signal is propagated through the first series of logic elements, and

wherein when the second input is selected, the carry signal is propagated through the second series of logic elements.

5. (Original) The logic circuit of claim 4, wherein the initialization circuit comprises:
 - a first initialization circuit connected to the first path; and
 - a second initialization circuit connected to the second path.
6. (Original) The logic circuit of claim 5, wherein the first initialization circuit comprises:
 - a second multiplexer connected to a selection signal, the multiplexer having;
 - a first input connected to a carry in signal;
 - a second input connected to a power supply; and
 - an output connected to the carry chain.
7. (Original) The logic circuit of claim 6, wherein the second initialization circuit comprises:
 - a logic gate connected to an end of the first path and a beginning of the second path.
8. (Original) The logic circuit of claim 6, wherein the second initialization circuit comprises:
 - a third input of the first multiplexer connected to a power supply.
9. (Currently Amended) A logic circuit comprising:
 - a first series of logic elements, each logic element having a look-up table and a dedicated adder to implement an arithmetic mode in the logic element;
 - a carry chain connecting the first series of logic element;

an initialization circuit connected to the carry chain to initialize the carry chain; and
an initialization value selection circuit connected to the initialization circuit, wherein the initialization value selection circuit is configured to generate a logic zero or a logic one as an initialization value for the initialization circuit, **the initialization value selection circuit further comprising:**

a logic gate connected to the initialization circuit; and
a multiplexer connected to the logic gate.

10. (cancelled)

11. (Currently Amended) The logic circuit of claim ~~10~~ 9, wherein the multiplexer includes one or more inputs.

12. (Currently Amended) A logic circuit comprising:

a first series of logic elements, each logic element having a look-up table and a dedicated adder to implement an arithmetic mode in the logic element;

a carry chain connecting the first series of logic element; and

an initialization circuit connected to the carry chain to initialize the carry chain, wherein the initialization circuit is disposed within the adder in a logic element;

wherein the dedicated adder includes:

an inverted carry input signal,

a non-inverted carry inputs signal, and

a non-inverted carry out signal, and

a multiplexer that generates the non-inverted carry out signal; and

wherein the initialization circuit includes;

a first logic gate connected to a first input of the multiplexer,

a second logic gate connected to second input of the multiplexer, and

wherein the first and second logic gates are connected to an initialization signal.

13. (cancelled)

14. (Original) The logic circuit of claim 12,

wherein the adder includes:

a non-inverted carry input signal,

an inverted carry out signal,

a first multiplexer that generates the inverted carry out signal,

and a second multiplexer that generates a sum; and

wherein the initialization circuit includes;

a third multiplexer with an output connected to a first input of the first multiplexer and an input connected to a second input of the first multiplexer,

a logic gate connected to the second multiplexer, and

wherein the third multiplexer and the logic gate are connected to an initialization signal.

15. (Original) The logic circuit of claim 12, further comprising;

a initialization value selection circuit connected to the initialization circuit, wherein the initialization value selection circuit is configured to allow selection of an initialization value for the initialization circuit.

16. (Original) The logic circuit of claim 15, wherein the initialization value can be set to a high or low value.

17. (Original) The logic circuit of claim 15, wherein the initialization value can be changed between a light value and a low value.

18. (Original) The logic circuit of claim 15,
wherein the adder includes;
a inverted carry input signal.
a non-inverted carry out signal, and
a first multiplexer that generates the non-inverted carry out signal; and
wherein the initialization circuit includes:
a second multiplexer having an output connected to a first input of the first
multiplexer,
a third multiplexer having an output connected to a second input of the first
multiplexer, and
wherein the first and second multiplexers are connected to an initialization signal
and the initialization value selection circuit; and
wherein the initialization value selection circuit includes:
a logic gate connected to the initialization circuit, and
a multiplexer connected to the logic gate.
19. (previously presented) A programmable logic device including the logic circuit of claim 2.
20. (previously presented) A digital system comprising a programmable logic device including the logic circuit of claim 2.
21. (Canceled)
22. (previously presented) A programmable logic device comprising:
an array of logic elements grouped into a plurality of logic blocks;

a first series of logic elements disposed within a logic block, each logic element having a look-up table and a dedicated adder to implement an arithmetic mode in the logic element;
a carry chain connecting the first series of logic element;
an initialization circuit connected to the carry chain to initialize the carry chain;
a first path connecting the first series of logic elements; and
a second path connecting a second series of logic elements,
wherein the logic elements in the first series are a subset of the logic elements in the second series.

23. (Original) The programmable logic device of claim 22, wherein the initialization circuit comprises:

a first initialization circuit connected to the first path; and
a second initialization circuit connected to the second path.

24. (Currently Amended) A programmable logic device comprising:

an array of logic elements grouped into a plurality of logic blocks;
a first series of logic elements disposed within a logic block, each logic element having a look-up table and a dedicated adder to implement an arithmetic mode in the logic element;
a carry chain connecting the first series of logic elements;
an initialization circuit connected to the carry chain to initialize the carry chain; ~~and~~
an initialization value selection circuit connected to the initialization circuit, wherein the initialization value selection circuit is configured to selection of an initialization value for the initialization circuit; and

wherein the initialization value can be set to a high or low value.

25. (cancelled)

26. (Original) The programmable logic device of claim 24, wherein the initialization value can be changed between a high value and a low value.

27. (currently amended) A programmable logic device comprising:
an array of logic elements grouped into a plurality of logic blocks;
a first series of logic elements disposed within a logic block, each logic element having a look-up table and a dedicated adder to implement an arithmetic mode in the logic element;
a carry chain connecting the first series of logic element; and
an initialization circuit connected to the carry chain to initialize the carry chain,
wherein the initialization circuit is disposed within the adder in logic element; **and**

wherein the adder includes:

an inverted carry input signal,

a non-inverted carry out signal, and

a multiplexer that generates the non-inverted carry out signal; and

wherein the initialization circuit includes:

a first logic gate connected to a first input of the multiplexer,

a second logic gate connected to a second input of the multiplexer, and

wherein the first and second logic gates are connected to an initialization signal.

28. (cancelled)

29. (Original) The programmable logic device of claim 27,
wherein the adder includes:

a non-inverted carry input signal,

an inverted carry out signal,

a first multiplexer that generates the inverted carry out signal,

a second multiplexer that generates a sum; and
wherein the initialization circuit includes:
a third multiplexer with an output connected to a first input of the first multiplexer
and an input connected to a second input of the first multiplexer,
a logic gate connected to the second multiplexer, and
wherein the third multiplexer and the logic gate are connected to an initialization
signal.

30. (Original) The programmable logic device of claim 27, further comprising:

an initialization value selection circuit connected to the initialization circuit, wherein the
initialization value selection circuit is configured to allow selection of an initialization value for
the initialization circuit.

31. (Original) The programmable logic device of claim 30,

wherein the adder includes:

a inverted carry input signal,
a non-inverted carry out signal, and
a first multiplexer that generates the non-inverted carry out signal; and

wherein the initialization circuit includes:

a second multiplexer having an output connected to a first input of the first
multiplexer,

a third multiplexer having an output connected to a second input of the first
multiplexer,

wherein the first and second multiplexers are connected to an initialization signal
and the initialization value selection circuit; and

wherein the initialization value selection circuit includes:

a logic gate connected to the initialization circuit, and
a multiplexer connected to the logic gate.

32. (previously presented) A digital system comprising a programmable logic device including the logic circuit of claim 22.

33. (Currently Amended) A method of initializing a carry chain in a programmable logic device, the method comprising:

implementing an arithmetic mode in a logic element using a dedicated adder in the logic element, wherein a series of logic elements are connected as carry chain;

initializing the carry chain using an initialization circuit connected to the carry chain; and

generating a logic zero or a logic one as an initialization value for the initialization circuit using an initialization value selection circuit connected to the initialization circuit, **the initialization value selection circuit further comprising:**

a logic gate connected to the initialization circuit; and

a multiplexer connected to the logic gate.